SEMICONDUCTORS / PROCESSORS

FEATURE

Multicore CPUs: Processor Proliferation

From multicore to many-core to hard-to-describe-in-a-single-word core

By ! MU"# $% M&& ' " / (!) U ! ' * +, --

Illustration: Frank Chimero

. his is /art of I" " " /ectrum's s/ecial re/ort: .o/ -- .echnologies of the 1ecade

Back in 1994, /rogrammers figured that whate2er code they wrote would run at least 3, /ercent faster on a -443 machine and 3, /ercent faster still on a 145 system% Coding would continue as it always had& with instructions designed to be e7ecuted one after the other%

But $unle &lukotun& then a newly minted /rofessor of electrical engineering at tanford& saw that the /arty couldn't go on fore2er% . he micro/rocessors of the day couldn't scale u/ as efficiently as you'd e7/ect through the mere addition of e2er more and e2er faster transistors& the two things that Moore's #aw /ro2ided%

.o sol2e that /roblem& &lukotun and his students designed the first general-/ur/ose multicore CPU% . his idea& more than any other in the /ast decade& is what has ke/t the semiconductor industry climbing the Moore's #aw /erformance cur2e% 8 ithout multicore chi/s& the com/uting ca/ability of e2erything from ser2ers to netbooks would not be much better than it was a decade ago% "2eryone's ha//y 9 e7ce/t /erha/s for the /rogrammers& who must now write code with threads of instructions that must be e7ecuted together 9 in /airs& :uartets& or e2en larger grou/ings%

It's not that old& single-core CPUs weren't already doing some /arallel /rocessing% 8 hen &lukotun began his work& most micro/rocessors had a ;su/erscalar; architecture% In the su/erscalar scheme& the CPU contained many re/licated com/onents& such as arithmetic units% Indi2idual instructions would be /arceled out to the waiting com/onents% caling u/ such ;instruction-le2el /arallelism; meant building in more and more such com/onents as the years rolled by%

&lukotun argued that within a few more generations& it wasn't going to be worth the effort% *ou needed to /ro2ide a :uadratic increase in resources for a linear increase in /erformance& he said& because of the com/le7ity of the logic in2ol2ed in /arceling out and kee/ing track of all the instructions% If you combined that with the delays inherent in the mess of interconnects among all those /arts& it seemed a losing /ro/osition% 1oug Burger and te/hen $eckler& both com/uter scientists at the Uni2ersity of .e7as& !ustin& /ut a finer /oint on it later in the decade& calculating that instead of the 3, /ercent im/ro2ements e2eryone had gotten used to& the com/uting industry should start thinking -+%3 /ercent% ! nd -+%3 /ercent isn't much of a reason to buy a new com/uter& is it<

&lukotun's answer was =ydra& a /rocessor whose /arallelism came not from redundant circuits within a single com/le7 CPU but from building four co/ies of a sim/ler CPU core on one chi/% . hat way& you sa2e on interconnects and on the time lost casting instructions out and reeling answers back in% In =ydra& you got /arallel /rocessing without all the delay-

inducing com/le7ity% In -44> ;we wra//ed u/ the hardware /ortion of the /ro?ect and declared 2ictory6; says &lukotun%

It was a :uiet 2ictory% In the com/uting en2ironment of the -44,s6 =ydra seemed a little craCy6 &lukotun says% u/erscalar designs were still deli2ering 3, /ercent /erformance im/ro2ements e2ery year% ;It was by no means clear at the time that our 2iew of the world was going to win6; he recalls% !nd indeed it would be years before /rocessor giants like Intel6 !d2anced Micro 1e2ices6 and IBM got the multicore religion &lukotun /reached% !nd when they did6 it would largely be for a reason he had hardly considered: /ower%

It turned out that the rising density of transistors on a chi/ intensified the hot s/ots in CPUs% .his6 e2en more than the resource-to-/erformance ratio that had bothered &lukotun6 was the /roblem that seemed most likely to sto/ Moore's #aw in its tracks% In /resentations in -444 and later6 Intel engineers showed that if trends in micro/rocessors were to continue6 by +,-, they'd burn as hot as the surface of the sun%

.he answer was clear: low down the CPU's clock and add more cores% .hat way6 you'd gain more from the e7tra /arallelism than you lost from the slower /rocessing% .he chi/ would gobble less /ower and generate less heat%

It was a daunting engineering ?ob6 but the big /rocessor makers were more /re/ared than you might e7/ect6 because they'd already redesigned the way that CPUs communicate with other chi/s% For Intel6 the solution6 called the front-side bus6 debuted in -4456 in the Pentium Pro% !ccording to Intel senior fellow te2e Pawlowski6 the bus was6 in large /art6 originally meant to sa2e on testing and 2alidation costs% It was a 2ery con2enient /iece of luck6 because when the time came to get two cores working together6 the front-side bus was there6 waiting to link them u/% !nd in +,,3 Intel released its first dual-core com/onent6 the Pentium 16 which was really two single-core chi/s in the same /ackage6 tied together by the front-side bus%

"ngineers at !M1 9influenced by &lukotun6 Burger6 and $eckler 9were more /ur/oseful% .hey /re//ed the initial6 single-core 2ersion of !M1's breakout ser2er chi/6 the &/teron6 with a redesigned communications com/onent that would make a multicore 2ersion easy% .hat 2ersion came out in +,,3% .he com/onent was the chi/'s ;northbridge6; a switchyard that acts as the chi/'s gateway to other chi/s in the com/uter%

IBM was6 arguably6 e2en more on to/ of the multicore re2olution% !round the same time that Intel's Pentium Pro was released6 the com/any began work on its Power@ /rocessor% #ooking for an ad2antage6 IBM entertained a number of cutting-edge ways to enhance instruction-le2el /arallelism in single cores6 according to (im $ahle6 chief architect of that design% But6 deciding to /lay it safe6 his team re?ected each% ;.urned out to be a good idea6; he says% .he most conser2ati2e o/tion was a dual-core /rocessor% !nd so Power@6 released in +,,-6 became the first mainstream com/uter /rocessor with more than one core on a single die%

&lukotun himself wasn't absent from the re2olution he /redicted% In +,,,6 he took the lessons from =ydra and founded !fara 8ebsystems% .hat start-u/ was ac:uired by un Microsystems in +,,+6 and its technology became un's /owerful 8eb ser2er CPU6 the eight-core Ultra /arc .- 0also known as) iagara56 released in +,,3%

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tanford Uni2ersity

&nce the multicore re2olution got going6 it had a natural momentum% ;!s soon as we got to two cores6 it became ob2ious we needed to start thinking about going to four6; says !M1 cor/orate fellow Chuck Moore% ;!nd as soon as we got to four6 we started thinking about going to si7 or eight%;

o today /rogrammers can again count on a solid 3, /ercent annual gain in effecti2e /rocessing /ower6 dri2en not by raw s/eed but by increasing /arallelism% .herein lies the rub% Back when &lukotun worked out =ydra6 ;it was unclear if you could take ad2antage of all the /arallelism6; he says% ;It's still unclear today%;

o where does it end< i7ty-four cores< !lready there% tart-u/ .ilera Cor/% is selling it 0see ;Com/any to 8atch;E% .wo hundred< &ne thousand< ;Cores are the new transistors6; ?okes &lukotun%

(ust adding traditional cores isn't going to be enough6 says !M1's Moore% .he scheme may ha2e sa2ed the /ower-2ersus-/erformance cur2e for a time6 but it won't do so fore2er% ;.hese days6 each core is only getting > or -, watts6; he says% ;In some sense we're running back into that /ower wall%; 8ith its new BulldoCer architecture6 !M1 has managed to buy some breathing room by finding a set of com/onents that the cores can share without seriously degrading their s/eed% But e2en so6 Moore's best guess is that -5 cores might be the /ractical limit for mainstream chi/s%

Intel's Pawlowski won't /ut a number on it6 but he will say that memory bandwidth between the cores is likely to be the big constraint on growth%

8hat will kee/ com/uting marching forward6 according to Moore6 is the integration of CPUs and gra/hics /rocessing units 0APUs5 into what !M1 calls an accelerated /rocessing unit6 or !PU% ay you want to brighten an image: (ust add - to the number re/resenting the brightness of e2ery /i7el% It'd be a waste of time to funnel all those bits single file through a CPU core6 or e2en -5 of them6 but APUs ha2e dedicated hardware that can transform all that data /ractically at once%

It turns out that many modern workloads ha2e ?ust that kind of data-le2el /arallelism% Basically6 you want to do the same thing to a whole lot of data%

.hat key insight dro2e !M1 to ac:uire a leading APU maker6 !.I .echnologies6 and start work on ?amming their two /roducts together% o a future /rocessor6 from !M1 at least6 would /robably contain multi/le CPU cores connected to se2eral APU elements that would ste/ in whene2er the work is of a ty/e that would gum u/ a CPU core%

8ith Cell6 the /rocessor released in +,,5 to /ower the Play tation B6 IBM has already gone in that direction% Instead of actual APU functions6 it de2elo/ed a more fle7ible core that s/eciali6es in e7ecuting the same instruction on se2eral /ieces of data at once% IBM6 with hel/ from .oshiba and ony6 stuck eight of the new cores on the same chi/ with a more traditional /rocessor core% But that's not :uite where $ahle6 who led the Cell /ro?ect6 sees things going in the future% Instead he e7/ects to see a mi7 of general-/ur/ose cores and cores s/eciali6ed for one task 9encry/tion6 decry/tion6 2ideo encoding6 decom/ression6 anything with a well-defined standard%

&lukotun agrees that such a heterogeneous mi7 of cores is the way forward6 but it's not going to be easy% ;It's going to make the /rogramming /roblem much worse than it is today6; he says% ;(ust as things were getting bad for software de2elo/ers6 they ha2e the /otential to get worse%; But don't worry% .hey're working on it%

For all of I""" /ectrum's .o/ -- .echnologies of the 1ecade6 2isit the s/ecial re/ort%

COMPANY TO WATCH:
Tile a C! "#,
San Jose, Calif.

In +,,>6 MI. /rofessor !nant !garwal transformed an academic /ro?ect to efficiently make use of lots of sim/le cores connected in a mesh into .ilera6 a com/any whose commercial /rocessor has one of the highest core counts of all% It's selling a 5@-core /roduct now6 the -,,-core .ile-A7 starts sam/le shi/ments in mid-+,,-6 and the com/any /lans a +,,-core /roduct in +,-B%